VISI Virtual Instruments™ Signal Integrity

Clock Analysis Software

To analyze jitter and ensure clock signal integrity with exceptional speed and accuracy, choose the Clock Analysis module for Virtual Instruments™ Signal Integrity (VISI) Software from *WAVECREST*. This powerful software package includes a complete set of characterization, debug and analysis tools for today's most demanding clock applications.

- **RJ and DJ separation for complete device characterization and analysis**
- **Viewing spectral components over a bandwidth**
- **User-definable filters to obtain RMS jitter over a bandwidth**
- **Estimation of total jitter for up to 10^{16} clock cycles in seconds**
- **Quantifying PLL response**
- **Test up to 10 channels for period jitter, skew and propagation delay**
- **Cycle-to-cycle jitter**
- **The Clock Analysis module is ideally suited to characterize and analyze the following devices:**
  - **— PLLs**
  - **— DLLs**
  - **— ring oscillators**
  - **— crystal oscillators**
  - **— clock trees**
  - **— SONET clocks**

Use the VISI Clock Analysis module in concert with the ***WAVECREST*** SIA-3000 to perform complete clock analysis in seconds. At this speed, you can test more devices in less time and accelerate time-to-market for your latest innovations. The Clock Analysis module can measure period, pulse width, cycle-to-cycle jitter, duty cycle distortion, propagation delay and skew. It can separate random jitter (RJ) and deterministic jitter (DJ), and quantify the magnitude and frequency of periodic modulations.

Quantify random and deterministic components

Period jitter provides information about system timing margins and short-cycle failures. The Clock Analysis module characterizes the magnitude of jitter on a clock signal or PLL by asynchronously measuring a histogram of periods, ensuring a valid statistical data set. Consider the bimodal histogram of period measurements from a 200 MHz clock (Fig. 1). The non-Gaussian shape of the histogram indicates a deterministic component arising from crosstalk, EMI or power supply noise. Using ***WAVECREST***'s patented TailFit™ algorithm, you can quantify the DJ and RJ components regardless of the shape of the histogram. Further analysis can be done to identify the periodic jitter using modulation analysis.

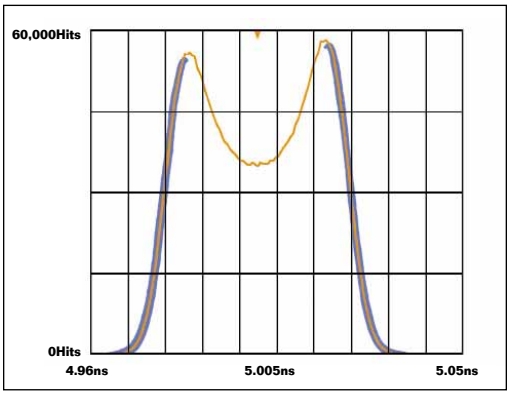

Fig. 1. This histogram of period measurements includes RJ and DJ components. Note how the Gaussian tails have been fitted to the left and right sides of the distribution to quantify RJ and DJ.

Perform modulation analysis

The Clock Analysis module offers modulation tools that make it easy to measure both the frequency and the amplitude of the DJ. First, an automated algorithm acquires period histograms over an increasing range of periods defined by the low-frequency cutoff. In the time domain, users can view the 1σ jitter values vs. span to obtain information about periodic jitter components, loop response or damping (see Fig. 2).

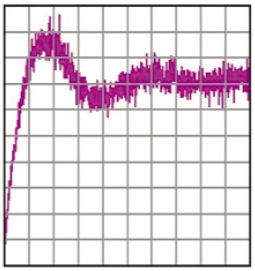

Fig. 2. The output from a PLL using the modulation tools. Note the jitter accumulation levels off; this indicates the PLL tracks the jitter above a certain span. This relates to a low frequency cutoff where any jitter below that frequency would be tracked by the PLL.

The ability to isolate the root cause of jitter is vital for thorough device characterization. A common source of DJ in clocks and PLLs is crosstalk, reflections and EMI (see Fig.1). The modulation tools in the Clock Analysis module also provide advanced debug and characterization capabilities that offer a spectral view of jitter (see Fig. 3). Different views of the FFT plot enable you to see cumulative amplitude of the interfering signal or its short-term cycle-to-cycle impact. The modulation tools also allow you to determine the precise frequency and magnitude of individual jitter components.

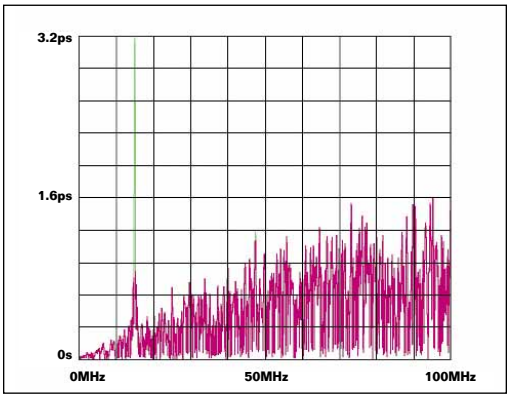

Fig. 3. The impact of spectral components on a single period. The plot shows a 15 MHz spectral component on a 200 MHz signal. Note the roll-off effect as the period reaches a lower frequency. Lower-frequency components of jitter have a lower impact on a single period.

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WAVECREST SIA-3000

- **Up to 10 parallel channels at 3 GHz/4.5 Gb/s**
- **Repeatable measurements with 200 fs resolution**
- **Multi-instrument functionality in the lab or production test**
- **Triggerless architecture**
- **The getting started wizard enables you to characterize period jitter, quantify RJ/DJ, and obtain a spectral view of jitter over a user-defined bandwidth at the touch of a button**

Analyze jitter as a function of voltage and temperature

All devices are designed to operate within a specific temperature and voltage range, requiring them to meet jitter specifications over the entire range. The Clock Analysis module provides a number of analysis tools to provide quantitative analysis and graphical views of the effects of a variable such as voltage or temperature. The composite plot tool, for example, simplifies viewing of voltage effects on period jitter. It allows you to overlay multiple plots onto a single plot, which clearly indicates the effect of voltage on period jitter (see Fig. 4).

Characterizing devices that are sensitive to temperature such as oscillators can be accomplished using the strip chart tool. With the strip chart tool, period histograms are acquired at regular time intervals as device temperature varies, which effectively tests for jitter as a function of temperature (see Fig. 5). You can also use the strip chart tool to observe the stability of the device as a function of time. Plus, the Clock Analysis module includes a waveform viewer that provides a graphical display of voltage and time characteristics of the signal.

Specialized tools for DRCG applications

For DRCG applications, the Clock Analysis module offers a Direct Rambus® Clock Generator validation tool that enables fast, accurate verification of Rambus® licensed DRCG modules. This tool measures timing characteristics for adjacent clock cycles of DRCG modules, as specified in the Rambus® DRCG validation specification (see Fig. 6). In fact, it performs all the DRCG verification tests in less than five seconds. Any DRCG module that is out of spec can be further diagnosed and debugged using the Clock Analysis module's comprehensive analytical toolset.

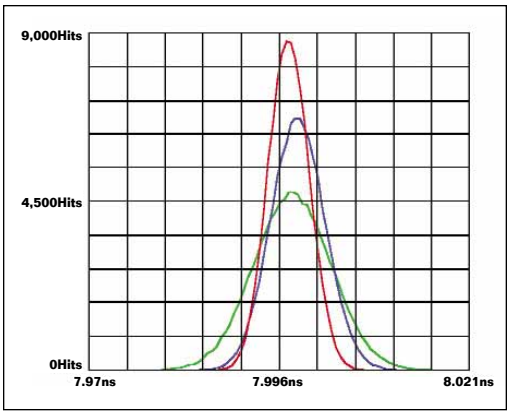

Fig. 4. Period histograms for a 125 MHz oscillator for different V_{dd} voltages, with 1σ jitter varying from 5.2 ps at 2.0V to 2.7 ps at 3.0V.

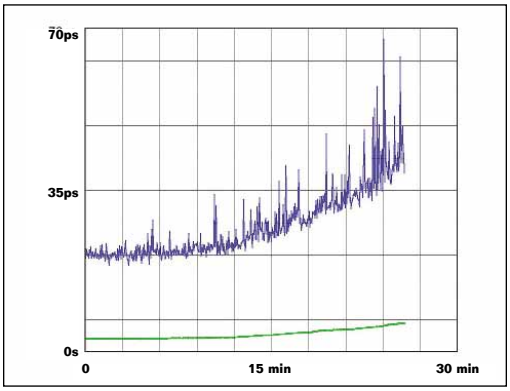

Fig. 5. Strip chart of the 1σ (green) and pk-pk (blue) jitter variation over a 30-minute time span during which oscillator temperature varied from 20° to 100° C. The 1σ values varied from 2.9 ps to 6.3 ps over the range. The pk-pk varied from 22 ps to 65 ps. Each data point in the series represents the statistic of histograms with 10,000 samples each, acquired every 0.1 seconds.

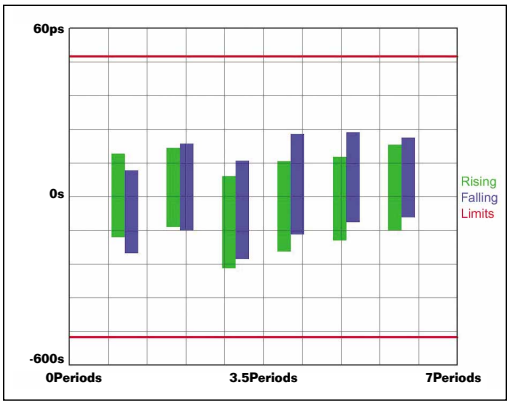

Fig. 6. DRCG validation tool showing adjacent cycle measurements for 1-6 cycle-to-cycle measurement for rising and falling edges. A summary table (not shown) is also generated, enabling you to "cut and paste" data into the Rambus DRCG template.

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